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### **Search Results -** Record(s) 1 through 10 of 16 returned.

1. Document ID: US 20030064578 A1

L4: Entry 1 of 16

File: PGPB

Apr 3, 2003

PGPUB-DOCUMENT-NUMBER: 20030064578

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20030064578 A1

TITLE: Method for fabricating semiconductor integrated circuit

PUBLICATION-DATE: April 3, 2003

INVENTOR - INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Nakamura, Yoshitaka	Tokyo		JP	
Tamaru, Tsuyoshi	Tokyo	:	JP	
Fukuda, Naoki	Tokyo		JP	*
Goto, Hidekazu	Tokyo		JP	
Asano, Isamu	Iruma-shi		JP	
Aoki, Hideo	Tokyo		JP	
Kawakita, Keizo	Tokyo		JP	
Yamada, Satoru	Tokyo		JP	
Tanaka, Katsuhiko	Tokyo		JP	
Sakuma, Hiroshi	Tokyo		JP	
Hirasawa, Masayoshi	Tokyo		JP	

US-CL-CURRENT: 438/627; 257/E21.648, 257/E23.145, 438/253, 438/643, 438/648

#### ABSTRACT:

[Object] To prevent Al wiring formed on a via-hole in which a CVD-TiN film is embedded from corroding.

[Constitution] A TiN film 71 and a W film 72 are deposited on a silicon oxide film 64 including the inside of a via-hole 66 by the CVD method and thereafter, the W film 72 and TiN film 71 on the silicon oxide film 64 are etched back to leave only the inside of the via-hole 66 and form a plug 73. Then, a TiN film 74, Al-alloy film 75, and Ti film 76 are deposited on the silicon oxide film 64 including the surface of the plug 73 by the sputtering method and thereafter, the Ti film 76, Al-alloy film 75, and TiN film 74 are patterned to form second-layer wirings 77 and 78.

Full	Title	Citation	n Front	Review	Classification	Date   R	eference	Sequences	Attachments	Claims	ROMC	Dra⊷ Desc	Image	
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2. Document ID: US 20030045086 A1

L4: Entry 2 of 16

File: PGPB

Mar 6, 2003

PGPUB-DOCUMENT-NUMBER: 20030045086

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20030045086 A1

TITLE: Semiconductor integrated circuit device and manufacturing method of semiconductor integrated circuit device

PUBLICATION-DATE: March 6, 2003

INVENTOR - INFORMATION:

STATE COUNTRY RULE-47 CITY NAME Noguchi, Junji Ome JP Ohashi, Naofumi Hanno JΡ Takeda, Kenichi Tokorozawa JP ďΡ Saito, Tatsuyuki Ome JΡ Akishima Yamaguchi, Hiruzu Ome JP Owada, Nobuo

US-CL-CURRENT: 438/621; 257/E21.304, 438/687

#### ABSTRACT:

After formation of Cu interconnections 46a to 46e each to be embedded in an interconnection groove 40 of a silicon oxide film 39 by CMP and then washing, the surface of each of the silicon oxide film 39 and Cu interconnections 46a to 46e is treated with a reducing plasma (ammonia plasma). Then, without vacuum break, a cap film (silicon nitride film) is formed continuously. This process makes it possible to improve the dielectric breakdown resistance (reliability) of a copper interconnection formed by the damascene method.

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	F000C	Draw Desc	Image

File: PGPB

3. Document ID: US 20030041878 A1

L4: Entry 3 of 16

PGPUB-DOCUMENT-NUMBER: 20030041878

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20030041878 A1

TITLE: Manufacturing method of semiconductor integrated circuit device

PUBLICATION-DATE: March 6, 2003

INVENTOR-INFORMATION:

CITY STATE COUNTRY RULE-47 NAME JP Shimada, Yutaka Chiyoda Mori, Yasuhiro Hitachinaka JР Morita, Koyo. Tachikawa JP JP Hitachinaka Yokoshima, Kenji

US-CL-CURRENT: <u>134/6</u>; <u>134/18</u>

#### ABSTRACT':

A foreign-matter removal capacity is improved in a <u>cleaning</u> process. When a wafer is cleaned while a <u>brush</u> is moved from the center of the wafer toward the outer circumference thereof, a discharge flow rate of <u>cleaning</u> liquid flowing into the <u>brush</u> is regulated so that the interval between the <u>brush</u> and the wafer is kept constant.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | MMC | Draw Desc | Image |

Mar 6, 2003

4. Document ID: US 20030032292 A1

L4: Entry 4 of 16

File: PGPB

Feb 13, 2003

PGPUB-DOCUMENT-NUMBER: 20030032292

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20030032292 A1

TITLE: Fabrication method of semiconductor integrated circuit device

PUBLICATION-DATE: February 13, 2003

INVENTOR - INFORMATION:

NAME

CITY

STATE

COUNTRY

RULE-47

Noguchi, Junji

Ome

JP

US-CL-CURRENT: 438/692; 257/E21.304, 438/690

ABSTRACT:

Provided is a fabrication method of a semiconductor integrated circuit device having a post-CMP cleaning apparatus equipped with at least two drying chambers downstream of a cleaning chamber. This makes it possible to dry wafers in parallel, thereby improving the through-put of the post-CMP cleaning.

Full	Title	Citation	Front	Review	Classitication	Date	Reference	Sequences	Attachments	ĺ

MAIC Draw Desc Image

5. Document ID: US 20030017419 A1

L4: Entry 5 of 16

File: PGPB

Jan 23, 2003

PGPUB-DOCUMENT-NUMBER: 20030017419

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20030017419 A1

TITLE: Mass production method of semiconductor integrated circuit device and manufacturing method of electronic device

PUBLICATION-DATE: January 23, 2003

INVENTOR - INFORMATION:

NAME CITY Fussa STATE COUNTRY

RULE-47

Futase, Takuya Saeki, Tomonori

Kashi, Mieko

Yokohama Yokohama ·

JΡ JΡ

JP

US-CL-CURRENT: 430/311; 257/E21.309, 430/330, 438/689, 438/745, 438/754, 438/758

#### ABSTRACT:

In order to prevent the contamination of wafers made of a transition metal in a semiconductor mass production process, the mass production method of a semiconductor integrated circuit device of the invention comprises the steps of depositing an Ru film on individual wafers passing through a wafer process, removing the Ru film from outer edge portions of a device side and a back side of individual wafers, on which said Ru film has been deposited, by means of an aqueous solution containing orthoperiodic acid and nitric acid, and subjecting said individual wafers, from which said Ru film has been removed, to a lithographic step, an inspection step or a thermal treating step that is in common use relation with a plurality of wafers belonging to lower layer

Jan 2, 2003

steps (an initial element formation step and a wiring step prior to the formation of a gate insulating film).

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | MMC | Draw Desc | Image |

| 6. Document ID: US 20030001277 A1

File: PGPB

PGPUB-DOCUMENT-NUMBER: 20030001277

PGPUB-FILING-TYPE: new

L4: Entry 6 of 16

DOCUMENT-IDENTIFIER: US 20030001277 A1

TITLE: Semiconductor integrated circuit device and manufacturing method of semiconductor integrated circuit device

PUBLICATION-DATE: January 2, 2003

INVENTOR-INFORMATION:

NAME CITY STATE COUNTRY RULE-47 Noguchi, Junji JΡ Ohashi, Naofumi JP Hanno Takeda, Kenichi Tokorozawa JP Saito, Tatsuyuki Ome JΡ Yamaguchi, Hiruzu JΡ Akishima Owada, Nobuo JΡ Ome

US-CL-CURRENT: <u>257/773</u>; <u>257/762</u>, <u>257/774</u>, <u>257/776</u>, <u>257/E21.304</u>, <u>438/280</u>, <u>438/629</u>, 438/687

#### ABSTRACT:

After formation of Cu interconnections 46a to 46e each to be embedded in an interconnection groove 40 of a silicon oxide film 39 by CMP and then washing, the surface of each of the silicon oxide film 39 and Cu interconnections 46a to 46e is treated with a reducing plasma (ammonia plasma). Then, without vacuum break, a cap film (silicon nitride film) is formed continuously. This process makes it possible to improve the dielectric breakdown resistance (reliability) of a copper interconnection formed by the damascene method.

	Full	Title	Citation	Front	Review	Classitication	Date	Reference	Sequences	Attachments		MMC	Draw Desc	Image		
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		7.	Docu	ment	ID: U	JS 20020	0946	591 A1					•			
L	4: E	ntry	7 of	16				•	File: P	GPB			J	ul 18	, 2002	2

PGPUB-DOCUMENT-NUMBER: 20020094691

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020094691 A1

TITLE: Method for manufacturing semiconductor device

PUBLICATION-DATE: July 18, 2002

INVENTOR - INFORMATION:

NAME CITY STATE COUNTRY RULE-47
Yokogawa, Kenetsu Tsurugashima JP
Momonoi, Yoshinori Kokubunji JP

Momonoi, Yoshinori Kokubunji JP
Tsujimoto, Kazunori Higashiyamato JP
Tachi, Shinichi Sayama JP

US-CL-CURRENT: 438/710

#### ABSTRACT:

Disclosed is a method for <u>manufacturing</u> a semiconductor device which efficiently carries out a process on a <u>semiconductor</u> substrate, such as dry etching, and <u>cleaning</u> for removing a foreign matter after the process. The method includes a step of removing a foreign matter by using both an electric action of a plasma generated by plasma generation means and a physical action caused by a frictional stress of a fast gas stream formed by a pad structure which is arranged close to a wafer surface.

Full 1	Title   Citation	Front Review	Classification   D	ate   Reference	Sequences	Attachments	KWIC	Draw Desc   Image	
		•							
 	***************************************								
1 8	B. Docu	ment ID: U	JS 2002009	92541 A1					

File: PGPB

L4: Entry 8 of 16

PGPUB-DOCUMENT-NUMBER: 20020092541

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020092541 A1

TITLE: Dry cleaning method

PUBLICATION-DATE: July 18, 2002

INVENTOR-INFORMATION:

STATE RULE-47 NAME CITY COUNTRY Yokoqawa, Kenetsu JP Tsurugashima JP Momonoi, Yoshinori Kokubunji Hino JP Izawa, Masaru ιTΡ Tachi, Shinichi Sayama

US-CL-CURRENT: <u>134/1.2</u>; <u>134/18</u>, <u>134/19</u>, <u>134/21</u>, <u>134/6</u>, <u>257/E21.226</u>

#### ABSTRACT:

There is disclosed a dry cleaning method capable of totally cleaning and removing particles left at the surfaces of the ultra fine structure of the semiconductor device within the vacuum state without being dependent on a wet cleaning method performed in the surrounding atmosphere. The dry cleaning method of the present invention is carried out such that each of the pads is approached to each of the front surface and the rear surface of a processed item such as the semiconductor wafer and the like, cleaning gas is injected into a fine clearance formed between both of them to generate a high-speed gas flow along the surface of the processed item and the particles left at the surfaces of the processed item are physically cleaned and removed with the high-speed gas flow. In order to assist this physical cleaning action, it is also possible to apply either a chemical cleaning method or an electrical cleaning method under application of plasma. In accordance with the dry cleaning method of the present invention, it is possible to attain the superior cleaning effect corresponding to the cleaning process performed under application of the prior art wet cleaning method without causing the processed to be exposed in the surrounding atmosphere.

Full Title Citation Front Review Classification Date Reference Sequences Attachments MMC Diaw Desc Image

Jul 18, 2002

9. Document ID: US 20020042193 A1

L4: Entry 9 of 16

File: PGPB

Apr 11, 2002

PGPUB-DOCUMENT-NUMBER: 20020042193

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020042193 A1

TITLE: Fabrication method of semiconductor integrated circuit device

PUBLICATION-DATE: April 11, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Noguchi, Junji	Ome		JP	
Asaka, Shoji	Hanno		JP	
Konishi, Nobuhiro	Ome		JP	
Ohashi, Naohumi	Hanno		JP	
Maruyama, Hiroyuki	Ome		JP	

US-CL-CURRENT: 438/618; 257/E21.576, 257/E21.579, 257/E21.582, 257/E21.584, 438/622, 438/677, 438/687

#### ABSTRACT:

The copper interconnect formed by the use of a damascene technique is improved in dielectric breakdown strength (reliability). During post-CMP cleaning, alkali cleaning, deoxidizing process due to hydrogen anneal or the like and acid cleaning are carried out in the order. After the post-CMP cleaning and before forming an insulation film for a cap film, hydrogen plasma and ammonia plasma processes are carried out on the semiconductor substrate. In this manner, a copper-based buried interconnect is formed in an interlayer insulation film structured of an insulation material having a low dielectric constant.

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments

MMC Draw Desc Image

10. Document ID: US 20010030367 A1

L4: Entry 10 of 16

File: PGPB

Oct 18, 2001

PGPUB-DOCUMENT-NUMBER: 20010030367

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20010030367 A1

TITLE: <u>Semiconductor integrated circuit device</u> and fabrication method for <u>semiconductor</u> integrated circuit device

PUBLICATION-DATE: October 18, 2001

INVENTOR - INFORMATION:

NAME CITY STATE COUNTRY RULE-47
Noguchi, Junji Ome JP
Ohashi, Naohumi Hannou JP
Saito, Tatsuyuki Ome JP

US-CL-CURRENT: 257/758; 257/E23.161, 438/622

ABSTRACT:

Cu interconnections embedded in an interconnection slot of a silicon oxide film are formed by polishing using CMP to improve the insulation breakdown resistance of a copper interconnection formed using the Damascene method, and after a post-CMP cleaning step, the surface of the silicon oxide film and Cu interconnections is treated by a reducing plasma (ammonia plasma). Subsequently, a continuous cap film (silicon nitride film) is formed without vacuum break.

Title   Citation   Front   Review   Classification   Date   Reference   Sequences   Attachments   KWC	Draw Desc Image
Generate Collection Print	
Term	Documents
ROTATING	1416508
ROTATINGS	13
(3 AND ROTATING).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	16
(L3 AND ROTATING).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	16

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# PALM INTRANET

Day: Thursday Date: 7/17/2003 Time: 11:59:48

# **Inventor Name Search Result**

Your Search was:

Last Name = SHIMADA

First Name = YUTAKA

Application#	Patent#	Status	Date Filed	Title	Inventor Name
10380578	Not Issued	020	03/14/2003	OPTICAL PICKUP ADJUSTING APPARATUS AND ADJUSTING METHOD	:
10363519	Not Issued	020	03/04/2003	OPTICAL PICKUP DEVICE, AND RECORDING AND/OR REPRODUCING DEVICE	SHIMADA, YUTAKA
10261458	Not Issued	030	10/02/2002	DEVICES FOR STORING AND ACCUMULATING DEFECT INFORMATION, SEMICONDUCTOR DEVICE AND DEVICE FOR TESTING THE SAME	SHIMADA, YUTAKA
10258467	Not Issued	020	03/18/2003	OBJECTIVE LENS DRIVE DEVICE, AND OPTICAL PICKUP DEVICE USING OBJECTIVE LENS DRIVE DEVICE	SHIMADA, YUTAKA
<u>10178592</u>	Not Issued	095	06/25/2002	METHOD FOR FABRICATING A MAGNETIC RECORDING MEDIUM	SHIMADA, YUTAKA
<u>10118966</u>	Not Issued	030	04/10/2002	TEST CIRCUIT FOR SEMICONDUCTOR MEMORY AND SEMICONDUCTOR MEMORY DEVICE	SHIMADA, YUTAKA
10083402	Not Issued	030	02/27/2002	MANUFACTURING METHOD OF SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE	SHIMADA, YUTAKA
<u>09914744</u>	Not Issued	041	09/04/2001	MAGNETIC SUBSTANCE WITH MAXIMUM COMPLEX PERMEABILITY	SHIMADA, YUTAKA
09826383	Not Issued	041	04/04/2001	ELECTROMAGNETIC NOISE SUPPRESSOR, SEMICONDUCTOR DEVICE	SHIMADA, YUTAKA

				USING THE SAME, AND METHOD OF MANUFACTURING THE SAME	
09580634	6339543	150	05/30/2000	WRITING METHOD FOR A MAGNETIC IMMOVABLE MEMORY AND A MAGNETIC IMMOVABLE MEMORY	SHIMADA, YUTAKA
09538701	6430143	150	03/30/2000	OPTICAL PICKUP DEVICE AND OPTICAL DISC RECORDING AND/OR REPRODUCING APPARATUS	SHIMADA, YUTAKA
.09459431	Not Issued	120	12/13/1999	COMPOSITE MAGNETIC MATERIAL AND ELECTROMAGNETIC INTERFERENCE SUPPRESSING USING THE SAME	SHIMADA, YUTAKA
<u>08823094</u> .	6055135	150	03/24/1997	EXCHANGE COUPLING THIN FILM AND MAGNETORESISTIVE ELEMENT COMPRISING THE SAME	SHIMADA , YUTAKA
08809220	Not Issued	161	05/12/1997	COMPOSITE MAGNETIC MATERIAL AND ELECTROMAGNETIC INTEFERENCE SUPPRESSOR MEMBER USING THE SAME	SHIMADA , YUTAKA
<u>08778920</u>	5837068	150	01/06/1997	MAGNETORESISTANCE EFFECT MATERIAL, PROCESS FOR PRODUCING THE SAME, AND MAGNETORESISTIVE ELEMENT	SHIMADA , YUTAKA
08714805	5827445	150	09/17/1996	COMPOSITE MAGNETIC ARTICLE FOR ELECTROMAGNETIC INTERFERENCE SUPPRESSOR	SHIMADA , YUTAKA
08580476	Not Issued	168	12/29/1995	MAGNETORESISTANCE EFFECT MATERIAL, PROCESS FOR PRODUCING THE SAME, AND MAGNETORESISTIVE ELEMENT	SHIMADA , YUTAKA
08527898	5752785	150	09/14/1995	DRAINAGE PUMP STATION AND DRAINAGE OPERATION METHOD FOR DRAINAGE PUMP STATION	SHIMADA , YUTAKA

08282745	Not Issued	168	07/29/1994	MAGNETORESISTANCE EFFECT MATERIAL, PROCESS FOR PRODUCING THE SAME, AND MAGNETORESISTIVE ELEMENT	SHIMADA , YUTAKA
08077602	5383984	250	06/17/1993	PLASMA PROCESSING APPARATUS ETCHING TUNNEL-TYPE	SHIMADA , YUTAKA
07984738	Not Issued	161	12/02/1992	SOFT MAGNETIC THIN FILM AND METHOD OF MANUFACTURING THE SAME	SHIMADA , YUTAKA
07536018	Not Issued	166	06/11/1990	SOFT MAGNETIC THIN FILM AND METHOD OF MANUFACTURING THE SAME	SHIMADA , YUTAKA
07498415	5135818	150	03/26/1990	THIN SOFT MAGNETIC FILM AND METHOD OF MANUFACTURING THE SAME	SHIMADA , YUTAKA
07314776	Not Issued	161	02/24/1989	METHOD OF TREATING AN OBJECT WITH PLASMAS	SHIMADA , YUTAKA
<u>07281349</u>	<u>4970435</u>	150	12/08/1988	PLASMA PROCESSING APPARATUS	SHIMADA , YUTAKA
06880346	Not Issued	161	06/25/1986	MULTILAYER COMPOSITE SOFT MAGNETIC MATERIAL COMPRISING AMORPHOUS AND INSULATING LAYERS AND A METHOD FOR MANUFACTURING THE CORE OF A MAGNETIC HEAD AND A REACTOR	SHIMADA , YUTAKA
06734827	4608297	150	05/17/1985	MULTILAYER COMPOSITE SOFT MAGNETIC MATERIAL COMPRISING AMORPHOUS AND INSULATING LAYERS AND A METHOD FOR MANUFACTURING THE CORE OF A MAGNETIC HEAD AND A REACTOR	SHIMADA , YUTAKA
06630900	4641213	150	07/16/1984	MAGNETIC HEAD	SHIMADA , YUTAKA
06630898	4609593	150	07/16/1984	MAGNETIC RECORDING MEDIUM	SHIMADA , YUTAKA
06630897	4557769	150	07/16/1984	SOFT MAGNETIC MATERIAL	SHIMADA , YUTAKA
06551340	Not Issued	161	11/14/1983	THIN-FILM MAGNETIC HEAD	SHIMADA,

					YUTAKA
06468794_	Not Issued	166	02/22/1983	MULTILAYER COMPOSITE	SHIMADA,
				SOFT MAGNETIC MATERIAL	YUTAKA
				COMPRISING AMORPHOUS	
				AND INSULATING LAYERS	
				AND A METHOD FOR	
				MANUFACTURING THE CORE	
				OF A MAGNETIC HEAD AND	
			,	A REACTOR	

Inventor Search Completed: No Records to Display.

	Last Name	First Name	•
Search Another:	shimada	yutaka	
Inventor		Search	

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### Search Results - Record(s) 31 through 40 of 40 returned.

31. Document ID: US 6167583 B1

L3: Entry 31 of 40

File: USPT

Jan 2, 2001

US-PAT-NO: 6167583

DOCUMENT-IDENTIFIER: US 6167583 B1

\*\* See image for Certificate of Correction \*\*

TITLE: Double side cleaning apparatus for semiconductor substrate

DATE-ISSUED: January 2, 2001

INVENTOR - INFORMATION:

NAME

CITY

STATE

ZIP CODE

COUNTRY

Miyashita; Naoto Abe; Masahiro Yokohama Yokohama JP JP

US-CL-CURRENT:  $\underline{15/77}$ ;  $\underline{134/172}$ ,  $\underline{134/199}$ ,  $\underline{134/95.2}$ ,  $\underline{15/102}$ ,  $\underline{15/302}$ ,  $\underline{15/88.3}$ 

#### ABSTRACT:

A double side <u>cleaning</u> apparatus includes a pair of roll-like <u>brushes</u> and at least one <u>cleaning brush</u>. The roll-like <u>brushes</u> are driven to rotate in <u>opposite</u> directions, and a semiconductor wafer is arranged between them in a non-contact manner. The <u>cleaning brush</u> is arranged near the pair of roll-like <u>brushes</u>. While the semiconductor wafer is arranged between the pair of roll-like <u>brushes</u> and its upper and lower surfaces are being cleaned, the <u>cleaning brush brushes</u> the side surface of the semiconductor wafer. A <u>cleaning agent</u> is supplied from the pair of roll-like <u>brushes</u> to the semiconductor wafer to clean it. Since the upper and lower surfaces of the semiconductor wafer are cleaned in a non-contact manner, dust can be removed efficiently (within a short period of time and a small space).

24 Claims, 12 Drawing figures Exemplary Claim Number: 1 Number of Drawing Sheets: 4

Full Title Citation Front Review Classification Date Reference Sequences Attachments

KNMC | Draw Desc | Image

32. Document ID: US 6028360 A

L3: Entry 32 of 40

File: USPT

Feb 22, 2000

US-PAT-NO: 6028360

DOCUMENT-IDENTIFIER: US 6028360 A

TITLE: Semiconductor integrated circuit device in which a conductive film is formed

over a trap film which in turn is formed over a titanium film

DATE-ISSUED: February 22, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP	CODE	COUNTRY
Nakamura; Yoshitaka	Ome			•	JP
Tamaru; Tsuyoshi	Hachiouji				JP
Fukuda; Naoki	Ome				JP
Goto; Hidekazu	Fussa				JP
Asano; Isamu	Iruma				JP
Aoki; Hideo	Musashi-murayama				JP
Kawakita; Keizo	Ome				JP
Yamada; Satoru	Ome				JP
Tanaka; Katsuhiko	Ome ·		•	·	JP
Sakuma; Hiroshi	Ome				JP
Hirasawa; Masayoshi	Ome				JP

US-CL-CURRENT: 257/758; 257/306, 257/310, 257/763, 257/E21.648, 257/E23.145

#### ABSTRACT:

The semiconductor device is formed according to the following steps. A TiN film 71 and a W film 72 are deposited on a silicon oxide film 64 including the inside of a via-hole 66 by the CVD method and thereafter, the W film 72 and TiN film 71 on the silicon oxide film 64 are etched back to leave only the inside of the via-hole 66 and form a plug 73. Then, a TiN film 74, Al-alloy film 75, and Ti film 76 are deposited on the silicon oxide film 64 including the surface of the plug 73 by the sputtering method and thereafter, the Ti film 76, Al-alloy film 75, and TiN film 74 are patterned to form second-layer wirings 77 and 78.

2 Claims, 56 Drawing figures Exemplary Claim Number: 1 Number of Drawing Sheets: 51

Full Title Citation Front Review Classification Date Reference Sequences Attachments

MVMC Draw Desc Image

33. Document ID: US 6022807 A

L3: Entry 33 of 40

File: USPT

Feb 8, 2000

US-PAT-NO: 6022807

DOCUMENT-IDENTIFIER: US 6022807 A

TITLE: Method for fabricating an integrated circuit

DATE-ISSUED: February 8, 2000

INVENTOR-INFORMATION:

NAME CITY STATE ZIP CODE COUNTRY

Lindsey, Jr.; Paul C. Lafayette CA McClelland; Robert J. San Ramon CA

US-CL-CURRENT: 438/693; 216/38, 257/E21.244, 257/E21.304, 438/690

#### ABSTRACT:

An apparatus 100 for removing surface non-uniformities is provided. This apparatus has a stage 103 for holding a substrate 127 to be processed. This substrate often includes a film thereon, where the film has the non-uniformities. The apparatus 200 includes a movable head 111, which can provide rotatable movement about a fixed axis 123. A drive motor 115 is operably attached to the movable head 111 to provide this rotatable movement. A pad 113 (e.g., polishing or planarizing pad) is attached to the movable head. This pad 113 comprises an abrasive material and also has a smaller length (e.g, diameter, etc.) relative to a length (e.g, diameter, etc.) of the substrate. The

smaller pad is capable of selectively removing a portion of the non-uniformities on the film.

19 Claims, 4 Drawing figures Exemplary Claim Number: 1 Number of Drawing Sheets: 4

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Affachments

IMMC Draw Desc Image

34. Document ID: US 5880024 A

L3: Entry 34 of 40

File: USPT

Mar 9, 1999

US-PAT-NO: 5880024

DOCUMENT-IDENTIFIER: US 5880024 A

TITLE: Semiconductor device having wiring self-aligned with shield structure and

process of fabrication thereof

DATE-ISSUED: March 9, 1999

INVENTOR-INFORMATION:

NAME CITY STATE ZIP CODE COUNTRY

Nakajima; Tsutomu Tokyo JP Hayashi; Yoshihiro Tokyo JP

US-CL-CURRENT: 438/669; 257/E21.257, 257/E21.582, 257/E23.144, 257/E23.154, 438/622,

438/633

ABSTRACT:

A <u>semiconductor integrated circuit device</u> has circuit components, a wiring arrangement electrically connected to the circuit components and a shield structure for preventing signal wirings from a cross-talk between the signal wirings, and the signal wirings are patterned from a conductive layer extending over grooves formed in the shield structure so as to be self-aligned with the shield structure.

5 Claims, 9 Drawing figures Exemplary Claim Number: 1 Number of Drawing Sheets: 6

Full Title Citation Front Review Classification Date Reference Sequences Attachments

1990 Draw Desc Image

35. Document ID: US 5598495 A

L3: Entry 35 of 40

File: USPT

Jan 28, 1997

US-PAT-NO: 5598495

DOCUMENT-IDENTIFIER: US 5598495 A

TITLE: Fiber optic connector housing, fiber optic receptacle, accessories employing

fiber optic connector housings and corresponding optical assemblies

DATE-ISSUED: January 28, 1997

INVENTOR-INFORMATION:

NAME CITY STATE ZIP CODE COUNTRY

Rittle; Jeffrey W. Endicott NY
Vetter; William W. Vestal NY
Webb; James R. Endicott NY

US-CL-CURRENT: 385/75; 385/76

#### ABSTRACT:

A new fiber optic connector housing and a new fiber optic receptacle, both of which conform to a new standard proposed by the X3T9.3 committee of the American National Standards Institute, are disclosed. In addition, four accessory devices for electro-optic modules, each of which includes one or more essentially conventional plug frames which fit into either one or more conventional, individual fiber optic connector housings or the new fiber optic connector housing, are disclosed.

11 Claims, 38 Drawing figures Exemplary Claim Number: 1 Number of Drawing Sheets: 18

Full	Title Citatio	n Front	Review	Classification		Attachments	FOMC	Draw Desc In	age

36. Document ID: US 5452388 A

L3: Entry 36 of 40 File: USPT Sep 19, 1995

US-PAT-NO: 5452388

DOCUMENT-IDENTIFIER: US 5452388 A

TITLE: Fiber optic connector housing, fiber optic receptacle, accessories employing

fiber optic connector housings and corresponding optical assemblies

DATE-ISSUED: September 19, 1995

INVENTOR-INFORMATION:

NAME CITY STATE ZIP CODE COUNTRY

Rittle; Jeffrey W. Endicott NY
Vetter; William W. Vestal NY
Webb; James R. Endicott NY

US-CL-CURRENT: 385/92; 385/89

#### ABSTRACT:

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A new fiber optic connector housing and a new fiber optic receptacle, both of which conform to a new standard proposed by the X3T9.3 committee of the American National Standards Institute, are disclosed. In addition, four accessory devices for electro-optic modules, each of which includes one or more essentially conventional plug frames which fit into either one or more conventional, individual fiber optic connector housings or the new fiber optic connector housing, are disclosed.

18 Claims, 38 Drawing figures Exemplary Claim Number: 1 Number of Drawing Sheets: 18

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Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	10000	Draw Des	c image
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37. Document ID: US 5325454 A

L3: Entry 37 of 40

File: USPT

Jun 28, 1994

US-PAT-NO: 5325454

DOCUMENT-IDENTIFIER: US 5325454 A

TITLE: Fiber optic connector housing

DATE-ISSUED: June 28, 1994

INVENTOR - INFORMATION:

NAME

CITY

STATE

ZIP CODE

COUNTRY

Rittle; Jeffrey W.

Endicott

NY

Vetter; William W.

Vestal

NY

Webb; James R.

Endicott

US-CL-CURRENT: 385/76; 385/77, 385/88, 385/89, 385/90

#### ABSTRACT:

A new fiber optic connector housing and a new fiber optic receptacle, both of which conform to a new standard proposed by the X3T9.3 committee of the American National Standards Institute, are disclosed. In addition, four accessory devices for electro-optic modules, each of which includes one or more essentially conventional plug frames which fit into either one or more conventional, individual fiber optic connector housings or the new fiber optic connector housing, are disclosed.

21 Claims, 38 Drawing figures Exemplary Claim Number: 1 Number of Drawing Sheets: 18

Full Title Citation Front Review Classification Date Reference Sequences Attachments

KMMC Draw Desc Image

38. Document ID: US 4689113 A

L3: Entry 38 of 40

File: USPT

Aug 25, 1987

US-PAT-NO: 4689113

DOCUMENT-IDENTIFIER: US 4689113 A

TITLE: Process for forming planar chip-level wiring

DATE-ISSUED: August 25, 1987

INVENTOR - INFORMATION:

NAME

CITY

STATE ZIP CODE

COUNTRY

Balasubramanyam; Karanam

Hopewell Junction

Dally; Anthony J.

Pleasant Valley

NY

Riseman; Jacob

Poughkeepsie

Ogura; Seiki

Hopewell Junction

US-CL-CURRENT: 438/631; 204/192.32, 257/750, 257/E21.025, 257/E21.583, 257/E21.585, 257/E21.587, 430/314, 430/315, 430/315, 430/317, 430/318, 438/670, 438/951, 438/963

#### ABSTRACT:

Disclosed is a process of forming high density, planar, single- or multi-level wiring for a semiconductor integrated circuit chip. On the chip surface is provided a dual layer of an insulator and hardened photoresist having various sized openings (grooves

for wiring and openings for contacts) therein in a pattern of the desired wiring. A conductive (e.g., metal) layer of a thickness equal to that of the insulator is deposited filling the grooves and contact openings. A sacrificial dual (lower and upper component) layer of (hardened) photoresist is formed filling the metal valleys and obtaining a substantially planar surface. The lower component layer is thin and conformal and has a higher etch rate than the upper component layer which is thick and nonconformal. By reactive ion etching the sacrificial layer is removed leaving resist plugs in the metal valleys. Using the plug as etch masks, the exposed metal is removed followed by removal of the remaining hardened photoresist layer and the plugs leaving a metal pattern coplanar with the insulator layer. This sequence of steps is repeated for multilevel wiring.

When only narrow wiring is desired, a single photoresist layer is substituted for the dual photoresist sacrificial layer.

21 Claims, 9 Drawing figures Exemplary Claim Number: 1 Number of Drawing Sheets: 2

Full Title Citation Front Review Classification Date Reference Sequences Attachments

RMC Draw Desc Image

39. Document ID: JP 2003068695 A

L3: Entry 39 of 40

File: JPAB

Mar 7, 2003

PUB-NO: JP02003068695A

DOCUMENT-IDENTIFIER: JP 2003068695 A

TITLE: MANUFACTURING METHOD OF SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

PUBN-DATE: March 7, 2003

INVENTOR-INFORMATION:

NAME

COUNTRY

SHIMADA, YUTAKA MORI, YASUHIRO MORITA, MITSUHIRO YOKOSHIMA, KENJI

INT-CL (IPC):  $\underline{H01} \ \underline{L} \ \underline{21/304}$ 

Full Title Citation Front Review Classification Date Reference Sequences Attachments

KWMC Draw Desc Image

40. Document ID: JP 2003068695 A US 20030041878 A1

L3: Entry 40 of 40

File: DWPI

Mar 7, 2003

DERWENT-ACC-NO: 2003-371428

DERWENT-WEEK: 200335

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TITLE: Semiconductor integrated circuit device manufacturing method involves cleaning wafer with demineralized water supplied from outside of <u>brush</u> while regulating quantity of water flowing into brush and wafer

INVENTOR: MORI, Y; MORITA, K; SHIMADA, Y; YOKOSHIMA, K

PRIORITY-DATA: 2001JP-0259111 (August 29, 2001)

PATENT-FAMILY:

PUB-NO JP 2003068695 A US 20030041878 A1 PUB-DATE

LANGUAGE

PAGES

MAIN-IPC

March 7, 2003 March 6, 2003 014 028 H01L021/304 B08B007/04

INT-CL (IPC):  $\underline{\text{B08}}$   $\underline{\text{B}}$   $\underline{7/04}$ ;  $\underline{\text{H01}}$   $\underline{\text{L}}$   $\underline{21/304}$ 

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1	Full	Title	Citation	Front	Review	Classitication	Date	Reference	Sequences	Attachments	KOMC	Draw Desc	Clip Ima	Image
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Term	Documents
BRUSH	172262
BRUSHES	54037
(2 AND BRUSH).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	40
(L2 AND BRUSH).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	40

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WEST	
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L3: Entry 39 of 40

File: JPAB

Mar 7, 2003

DOCUMENT-IDENTIFIER: JP 2003068695 A

TITLE: MANUFACTURING METHOD OF SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

Abstract Text (1):

PROBLEM TO BE SOLVED: To improve foreign matter removing performance in a cleaning processing.

Abstract Text (2):

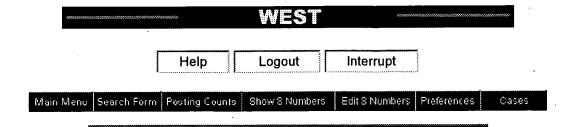
SOLUTION: In cleaning a wafer 2, while moving a brush 7 from the center toward outer periphery of the wafer 2, discharge flow rates X1, X2 of a cleaning liquid to be made to flow are adjusted, so that distances d1, d2 between the brush 7 and the wafer 2 become constant.

# **WEST Search History**

DATE: Thursday, July 17, 2003

Set Name side by side		Hit Count	Set Name result set
DB=U	SPT,PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=ADJ		
L5	(134/6 OR 134/33 OR 134/902).CCLS. and 12	5 -	L5
L4	L3 and rotating	16	L4
L3	L2 and brush	40	L3 .
L2	L1 and cleaning	370	L2
L1	manufacturing and (semiconductor integrated circuit device)	4847	L1

END OF SEARCH HISTORY



# Search Results -

Term	Documents
134/6	1161
134/6S	0
134/33	539
134/33S	0
134/902	1968
134/902S	0
(((134/33 OR 134/6 OR 134/902).CCLS.) AND 2).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	5
((134/6 OR 134/33 OR 134/902).CCLS. AND L2).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	5

Database: Search:	US Patents Full-Text Database US Pre-Grant Publication Full-Text Database JPO Abstracts Database EPO Abstracts Database Derwent World Patents Index IBM Technical Disclosure Bulletins  L5  Refine Search  Recall Text  Clear
	Search History

DATE: Thursday, July 17, 2003 Printable Copy Create Case

Set Name side by side		Hit Count	Set Name result set
DB = US	SPT,PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=ADJ		
<u>L5</u>	(134/6 OR 134/33 OR 134/902).CCLS. and 12	5	<u>L5</u>
` <u>L4</u>	L3 and rotating	16	<u>L4</u>
<u>L3</u>	L2 and brush	40	<u>L3</u>
<u>L2</u> · .	L1 and cleaning	370	<u>L2</u>
<u>L1</u>	manufacturing and (semiconductor integrated circuit device)	4847	<u>L1</u>

# **END OF SEARCH HISTORY**

## WEST

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### Search Results - Record(s) 11 through 16 of 16 returned.

11. Document ID: US 6586161 B2

L4: Entry 11 of 16

File: USPT

Jul 1, 2003

US-PAT-NO: 6586161

DOCUMENT-IDENTIFIER: US 6586161 B2

TITLE: Mass production method of semiconductor integrated circuit device and

manufacturing method of electronic device

DATE-ISSUED: July 1, 2003

INVENTOR-INFORMATION:

NAME CITY STATE ZIP CODE COUNTRY

Futase; Takuya Fussa JP
Saeki; Tomonori Yokohama JP
Kashi; Mieko Yokohama JP

US-CL-CURRENT: 430/311; 216/83, 427/250, 427/252, 427/253, 427/576, 430/330, 438/405, 438/459

ABSTRACT:

In order to prevent the contamination of wafers made of a transition metal in a semiconductor mass production process, the mass production method of a semiconductor integrated circuit device of the invention comprises the steps of depositing an Ru film on individual wafers passing through a wafer process, removing the Ru film from outer edge portions of a device side and a back side of individual wafers, on which said Ru film has been deposited, by means of an aqueous solution containing orthoperiodic acid and nitric acid, and subjecting said individual wafers, from which said Ru film has been removed, to a lithographic step, an inspection step or a thermal treating step that is in common use relation with a plurality of wafers belonging to lower layer steps (an initial element formation step and a wiring step prior to the formation of a gate insulating film).

46 Claims, 35 Drawing figures Exemplary Claim Number: 1 Number of Drawing Sheets: 22

Full	Titte	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments

RMC Draw Desc Image

12. Document ID: US 6509273 B1

L4: Entry 12 of 16

File: USPT

Jan 21, 2003

US-PAT-NO: 6509273

DOCUMENT-IDENTIFIER: US 6509273 B1

TITLE: Method for manufacturing a semiconductor device

DATE-ISSUED: January 21, 2003

INVENTOR - INFORMATION:

ZIP CODE COUNTRY CITY STATE NAME JP Imai; Toshinori Ome JΡ Ohashi; Naofumi Hanno JΡ Homma; Yoshio. Hinode JΡ Kokubunji Kondo; Seiichi

US-CL-CURRENT: 438/693; 438/691

#### ABSTRACT:

Problematic dishing and erosion in forming embedded metal interconnection by a chemical mechanical polishing (CMP) method are suppressed.

Formation of embedded Cu interconnects 46a to 46e by chemical mechanical polishing of a Cu film 46 formed in interconnect trenches 40 to 44 is performed by abrasive-grain-free chemical mechanical polishing using a polishing liquid of an abrasive grain content less than 0.5 wt % (CMP of the first step); with-abrasive-grain chemical mechanical polishing using a polishing liquid of an abrasive grain content of 0.5 or more wt % (CMP of the second step); and selective chemical mechanical polishing using a polishing liquid to which an anticorrosive such as benzotriazole (BTA) is added (CMP of the third step).

45 Claims, 31 Drawing figures Exemplary Claim Number: 1 Number of Drawing Sheets: 25

Full Title Citation Front Review Classification Date Reference Sequences Affachments 1996	C Draw De

13. Document ID: US 6492730 B1

L4: Entry 13 of 16

File: USPT

Dec 10, 2002

US-PAT-NO: 6492730

DOCUMENT-IDENTIFIER: US 6492730 B1

TITLE: Method for fabricating semiconductor integrated circuit

DATE-ISSUED: December 10, 2002

INVENTOR-INFORMATION:

INVENTOR INCOMENTATION.		0			
NAME	ĊITY	STATE	ZIP	CODE	COUNTRY
Nakamura; Yoshitaka	Ome ·				JP
Tamaru; Tsuyoshi	Hachiouji				JP
Fukuda; Naoki	Ome			•	JP
Goto; Hidekazu	Fussa				JP
Asano; Isamu	Iruma				JР
Aoki; Hideo	Musashi-murayama				JP
Kawakita; Keizo	Ome				JP
Yamada; Satoru	Ome				JP ·
Tanaka; Katsuhiko	Ome				JP
Sakuma; Hiroshi	Ome				JP
Hirasawa; Masayoshi	Ome				JP

US-CL-CURRENT: <u>257/758</u>; <u>257/306</u>, <u>257/310</u>, <u>257/763</u>, <u>257/E21.648</u>, <u>257/E23.145</u>

#### ABSTRACT:

The semiconductor device is formed according to the following steps. A TiN film 71 and a W film 72 are deposited on a silicon oxide film 64 including the inside of a via-hole

66 by the CVD method and thereafter, the W film 72 and TiN film 71 on the silicon oxide film 64 are etched back to leave only the inside of the via-hole 66 and form a plug 73. Then, a TiN film 74, Al-alloy film 75, and Ti film 76 are deposited on the silicon oxide film 64 including the surface of the plug 73 by the sputtering method and thereafter, the Ti film 76, Al-alloy film 75, and TiN film 74 are patterned to form second-layer wirings 77 and 78.

10 Claims, 56 Drawing figures Exemplary Claim Number: 1 Number of Drawing Sheets: 51

Full Title Citation Front Review Classification Date Reference Sequences Affachments

KAMC Draw Desc Image

14. Document ID: US 6167583 B1

L4: Entry 14 of 16

File: USPT

Jan 2, 2001

US-PAT-NO: 6167583

DOCUMENT-IDENTIFIER: US 6167583 B1

\*\* See image for Certificate of Correction \*\*

TITLE: Double side cleaning apparatus for semiconductor substrate

DATE-ISSUED: January 2, 2001

INVENTOR-INFORMATION:

NAME CITY STATE ZIP CODE COUNTRY

Miyashita; Naoto Yokohama JP Abe; Masahiro Yokohama JP

US-CL-CURRENT: 15/77; 134/172, 134/199, 134/95.2, 15/102, 15/302, 15/88.3

#### ABSTRACT:

A double side <u>cleaning</u> apparatus includes a pair of roll-like <u>brushes</u> and at least one <u>cleaning brush</u>. The roll-like <u>brushes</u> are driven to rotate in <u>opposite</u> directions, and a <u>semiconductor</u> wafer is arranged between them in a non-contact manner. The <u>cleaning brush</u> is arranged near the pair of roll-like <u>brushes</u>. While the <u>semiconductor</u> wafer is arranged between the pair of roll-like <u>brushes</u> and its upper and lower surfaces are being cleaned, the <u>cleaning brush brushes</u> the side surface of the <u>semiconductor</u> wafer. A <u>cleaning</u> agent is <u>supplied from the pair of roll-like brushes</u> to the <u>semiconductor</u> wafer to clean it. Since the upper and lower surfaces of the <u>semiconductor</u> wafer are cleaned in a non-contact manner, dust can be removed efficiently (within a short period of time and a small space).

24 Claims, 12 Drawing figures Exemplary Claim Number: 1 Number of Drawing Sheets: 4

Full Title Citation Front Review Classification Date Reference Sequences Attachments

KWMC | Drawn Desc | Image

15. Document ID: US 6028360 A

L4: Entry 15 of 16

File: USPT

Feb 22, 2000

US-PAT-NO: 6028360

DOCUMENT-IDENTIFIER: US 6028360 A

TITLE: Semiconductor integrated circuit device in which a conductive film is formed

over a trap film which in turn is formed over a titanium film

DATE-ISSUED: February 22, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Nakamura; Yoshitaka	Ome			JP
Tamaru; Tsuyoshi	Hachiouji			JP
Fukuda; Naoki	Ome <sup>J</sup>			JP
Goto; Hidekazu	Fussa			JP
Asano; Isamu	Iruma			JP
Aoki; Hideo	Musashi-murayama			JP
Kawakita; Keizo	Ome			JP
Yamada; Satoru	Ome			JP
Tanaka; Katsuhiko	Ome		•	JP
Sakuma; Hiroshi	Ome			JP
Hirasawa; Masayoshi	Ome			JP

US-CL-CURRENT: 257/758; 257/306, 257/310, 257/763, 257/E21.648, 257/E23.145

#### ABSTRACT:

The semiconductor device is formed according to the following steps. A TiN film 71 and a W film 72 are deposited on a silicon oxide film 64 including the inside of a via-hole 66 by the CVD method and thereafter, the W film 72 and TiN film 71 on the silicon oxide film 64 are etched back to leave only the inside of the via-hole 66 and form a plug 73. Then, a TiN film 74, Al-alloy film 75, and Ti film 76 are deposited on the silicon oxide film 64 including the surface of the plug 73 by the sputtering method and thereafter, the Ti film 76, Al-alloy film 75, and TiN film 74 are patterned to form second-layer wirings 77 and 78.

2 Claims, 56 Drawing figures Exemplary Claim Number: 1 Number of Drawing Sheets: 51

Full Title	Citation Fr	ont Review	Classification	Date	Reference	Sequences	Attachments

KMC Draw Desc Image

16. Document ID: US 6022807 A

L4: Entry 16 of 16

File: USPT

Feb 8, 2000

US-PAT-NO: 6022807

DOCUMENT-IDENTIFIER: US 6022807 A

TITLE: Method for fabricating an integrated circuit

DATE-ISSUED: February 8, 2000

INVENTOR-INFORMATION:

NAME CITY STATE ZIP CODE COUNTRY

Lindsey, Jr.; Paul C. Lafayette CA McClelland; Robert J. San Ramon CA

US-CL-CURRENT: 438/693; 216/38, 257/E21.244, 257/E21.304, 438/690

#### ABSTRACT:

An apparatus 100 for removing surface non-uniformities is provided. This apparatus has a stage 103 for holding a substrate 127 to be processed. This substrate often includes a film thereon, where the film has the non-uniformities. The apparatus 200 includes a

movable head 111, which can provide rotatable movement about a fixed axis 123. A drive motor 115 is operably attached to the movable head 111 to provide this rotatable movement. A pad 113 (e.g., polishing or planarizing pad) is attached to the movable head. This pad 113 comprises an abrasive material and also has a smaller length (e.g, diameter, etc.) relative to a length (e.g, diameter, etc.) of the substrate. The smaller pad is capable of selectively removing a portion of the non-uniformities on the film.

19 Claims, 4 Drawing figures Exemplary Claim Number: 1 Number of Drawing Sheets: 4

Full Title Citation Front Review Classification Date Reference Sequences Attachments Milit Draw Desc Image
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Term	Documents
ROTATING	1416508
ROTATINGS	13
(3 AND ROTATING).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	. 16
(L3 AND ROTATING).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	16

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